REMARKS

This responds to the Office Action mailed on April 4, 2006. Reconsideration is respectfully requested.

Claims 1 – 7, 9 – 15, 17, 19 – 22 and 24 – 26 are amended, claim 8 is canceled, and claims 27 - 28 are added; as a result, claims 1 – 7 and 9 - 28 are now pending in this application. Claims 24 – 26 are withdrawn from consideration.

Objections to the Specification

The specification was objected to due to informalities. It is believed that the amendments made herein to the specification obviate said objections. Applicant would like to thank the Examiner for noting these informalities in Applicant's specification.

In the Drawing

The drawings were objected to for not showing every feature of the invention. It is believed that the amendments made herein to the drawings obviate said objections. In particular, the embodiment claimed in claim 8 in which the regular and supplemental voltage supplies are provided by a single voltage source and in which the regular voltage supply is decoupled from the supplemental voltage supply during the standby mode. Claim 8 has been cancelled negating the requirement that this feature be shown in the drawings. Applicant therefore believes that the objection to the drawings has been overcome.

FIG. 4 has been amended to properly show the current path through the well of FET 432 from supplemental supply voltage (node 434) that occurs during standby mode. Well 540 and well tap 538 are also now shown. These amendments are described in more detail below. No new matter has been introduced by the amendment to FIG. 4

Objections to the Claims

Claims 1-19 were objected to due to informalities. The word 'circuitry' in 'data-retention circuitry' has been changed to 'circuit'. In claim 6, the phrase 'one of' has been deleted. In claim 7, the antecedent basis for 'sleep signal' and 'well-tap' has been corrected. Withdrawn claims 24 – 26 have been amended to correct typographical errors noted.

§112 Rejection of the Claims

Claims 1-23 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1 – 23 have been rejected because it was not understood by the Examiner what is meant by "through a well tap" in each independent claim.

The independent claims 1, 12, 20 and 24 have been amended in accordance with the description of Applicant's specification to recite 1) that the well tap comprises a conductive path to a resistive well of the semiconductor die, and 2) that leakage current of the data-retention subcircuits is drawn through the well tap from the supplemental voltage supply during standby mode.

FIG. 4 has also been amended in accordance with the Applicant's specification to correctly show the current path for leakage current during sleep mode. As amended, FIG. 4 shows connection from the supplemental supply voltage (node 434) to well 540 of FET 432, and shows a current path from well 540 of FET 432 through well tap 538 to data-retention subcircuits 424 and 426. Well tap 538 and well 540 of amended FIG. 4 may correspond to well tap 538 and well 540 of FIG. 5. As can be seen, current may flow from the supplemental supply voltage (node 434) to well 540, and current may also flow from well 540 to data-retention subcircuits 424 and 426.

The prior FIG. 4 erroneously showed a direct connection from the supplemental supply voltage (node 434), the well of FET 432, and data-retention subcircuits 424 and 426. Support for this amendment to FIG. 4 and the amendment to the claims may be found throughout Applicant's specification, and particularly on page 11 lines 15 – 26, page 12 lines 20 – 32, and page 13 lines 1 – 15.

In view of the amendment to claims 1, 12, and 20, and in view of the amendment to FIG. 4, Applicant submits that the rejection of claims 1-23 were rejected under 35 U.S.C. § 112, second paragraph, has been overcome.

Allowable Subject Matter

Claims 11 and 19 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, second paragraph, set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

The recitations of claims 11 and 19 have been rewritten as new independent claims 27 and 28 respectively and include the limitations of the base claim and all intervening claims. Claims 27 and 28 also recite that the well tap comprises a conductive path to a well of the semiconductor die. Claims 27 and 28 also include recitations to clarify the operation of the supply-switching subcircuit as discussed below. Based on these recitations, Applicant submits that the rejections under 35 U.S.C. § 112, second paragraph have been overcome and that claims 27 and 28 are in condition for allowance.

Claims 11 and 19 have been amended to depend from claims 1 and 12 respectively and to recite an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal. Claims 11 and 19 also recite that the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and that the pass-gate subcircuit comprises higher-leakage semiconductor devices. Claims 11 and 19 also recite that the lower-leakage devices having at least one of a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

The use of lower-leakage devices for the data-retention subcircuits allows a small amount of current to be drawn through the resistive well of the semiconductor die. The use of higher-leakage devices may result in excessive voltage drop through the resistive well making it difficult for the devices to retain their state in standby mode.

Applicant submits that the recitations of claims 11 and 19 are not taught, suggested or motivated by any of the cited references.

§*103 Rejection of the Claims*

Claims 1, 3, 7, 12, 14 and 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over either Stan et al. (U.S. 6,538,471) or Ooishi (U.S. 6,535,433) in view of any one of Levinson (U.S. 5,880,623), Notani et al. (U.S. 6,556,071) Ooishi (U.S. 5,801,576), Mulatti et al. (U.S. 6,307,396) and Bhavnagarwala et al. (U.S. 6,977,519).

Claims 2, 4, 5, 6, 8-10, 13, 15-18 and 23 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over either Stan et al. or Ooishi '433 in view of any one of Levinson, Notani et al., Ooishi '576, Mulatti et al., and Bhavnagarwala et al. and further in view of Ogawa (U.S. 6,246,265).

Applicant's claim 1 is directed to a data-retention circuit comprising data-retention subcircuits and a supply-switching subcircuit. As recited in claim 1, the supply-switching subcircuit decouples the data-retention subcircuits from the regular voltage supply to allow leakage current of the data-retention subcircuits to be drawn through a well tap from a supplemental voltage supply during a standby mode. Claim 1, as amended, also recites that the well tap couples the data-retention subcircuits to a resistive well of a semiconductor die allowing the data-retention circuitry to draw the leakage current through a resistive well of a semiconductor die during standby mode. As further recited in claim 1, the well tap comprises a conductive path to the resistive well of the semiconductor die. Independent claims 12 and 20 recite similar limitations.

Support for these amendments may be found throughout Applicant's specification, and particularly on page 9 lines 20 – 22, page 11 lines 15 – 26, page 12 lines 20 – 32, and page 13 lines 1 – 15.

Applicant submits that none of the cited references teach, suggest or motivate any of the following recitations:

1) The use of leakage current of semiconductor devices to retain state during standby mode;

2) A well tap to allow the leakage current to flow from a resistive well of the semiconductor die to allow semiconductor devices to retain their state;

3) A well tap comprising a conductive path to the resistive well of the semiconductor die; and

4) Decoupling data-retention devices from a regular voltage supply during standby mode to allow the devices to draw leakage current during standby mode so as to retain their state.

Stan (471) has been cited by the Examiner for disclosing a master-slave latch with cross-coupled inverters and a sleep mode. Stan, as stated by the Examiner, does not disclose the use of different power supplies during standby mode.

Ooishi (433) has been cited by the Examiner for disclosing a master-slave latch with cross-coupled inverters and a sleep mode. Ooishi (433) uses different power sources from the master and slave portions of the flip-flop (see FIG. 4 of Ooishi). The power supplies in Ooishi couple directly to either the drain or source of the FETs. There is no indication in Ooishi that any current is supplied to slave 24 through a well of a semiconductor device. Furthermore, there is no teaching in Ooishi currently supplied to slave 24 is limited to leakage current.

The Examiner cites Levinson, Notani et al., Ooishi (576), Mulatti and Bhavnagarwala for disclosing the use of separate voltage/power supplies. Applicant submits that none of these references teach, suggest or motivate the use of leakage current of data-retention devices to retain state during standby mode. Furthermore, Applicant submits that none of these references teach, suggest or motivate a well tap comprising a conductive path coupling the data-retention devices to a resistive well of a semiconductor die to the data-retention devices to draw leakage current from the resistive well the semiconductor die to allow the devices to retain their state.

Applicant points out that although the well is resistive, the leakage current may be small enough so that a slight voltage drop across the resistive well would not affect the ability of the data-retention devices to retain their state.

In Levinson, the voltage VDD is used when FET M2 is cut off. In Notani, voltage VA1 is used while FET AQ3 is cut off. In Mulatti, a voltage on capacitor C1 is used when FETs MP1 and MP2 are cut off. In Bhavnagarwala, voltage PMOS BULK is used when FET M6 is cut off. In Ooishi (576), voltage VC is used when FET PW is cut off. In no case is any of the current or voltage supplied through a resistive n well of a semiconductor die. Furthermore, in no case are

data-retention elements coupled to a resistive well through a well tap of a semiconductor die as recited in Applicant claims.

In view of the above, Applicant submits that claims 1, 12 and 20 are allowable over the cited references.

Applicant's claims 2, 13 and 21 further distinguish over Stan and Ooishi (433) by reciting that the isolation subcircuit and the data-retention subcircuits are outside a data path operable when voltage from the regular voltage supply is present. In Stan, data retention devices G3 and G4 are part of the direct data path during normal operations (see Stan FIG. 2). In Ooishi (433), the data signal path for output at element 25b is provided through the data retention elements of slave 24 (see Ooishi (433) FIG. 4).

Claim 9 further distinguishes over Stan by reciting separate master and slave latches in which signals are provided from the master latch to the pass gate subcircuit and then to the isolation subcircuit. In Stan, the functions a master and slave latch are combined into a single non-separable circuit 20 (see Stan FIG. 2).

Claims 3, 14 and 22, as amended, further distinguish over the cited references by reciting that the data-retention subcircuits and supply-switching subcircuits comprise semiconductor devices fabricated on the semiconductor die, and that leakage current provided through the well tap comprises primarily leakage current of the semiconductor devices comprising the data-retention subcircuits. Applicant finds no teaching, suggestion or motivation of these recitations in Stan, Ooishi (433), Levinson, Notani et al., Ooishi (576), Mulatti or Bhavnagarwala.

In view of the above, Applicant submits that the rejection of claims 1 – 10, 12 – 18 and 20 – 23 under 35 U.S.C. § 103(a) has been overcome.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((480) 659-3314) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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